Remarks

No Claims are amended. No new claims are added. Claims 1-94 are pending for consideration. In view of the following amendments and remarks, Applicant respectfully requests that this application be allowed and forwarded on to issuance.

Statement of Substance of Interview Dated January 25th, 2007

Applicant wishes to thank Examiner Nadia Khoshnoodi for conducting a telephonic interview with Applicant's attorney, Daniel T. McGinnity, on January 25th, 2007. During the interview, Applicant's attorney submitted patentability arguments with respect to the cited references, and with specific discussion of Nason and Garcia, including that:

- The references of record fail to disclose, teach, or suggest "at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis" as recited for example in claim 1.
- The references of record fail to disclose, teach, or suggest "a cryptographic processor that resides on the video card" as recited for example in claim 1.
- The Garcia reference is non-enabling with respect to "a cryptographic processor that resides on the video card" for which it is relied upon.
- The references teach away from the proposed combination.
- The proposed combination lacks motivation at least because it would change the principle of operation of the Nason reference.

For at least theses reasons, Applicant submits that the Office has not established a *prima facie* case of anticipation or obviousness with respect to the pending claims. While no agreement was reached, the Examiner indicated that the patentability arguments would be reconsidered if submitted in writing. Accordingly, the following remarks incorporate the patentability arguments which were discussed during the interview. In the spirit of cooperation, Applicant

requests that, if any issues remain upon reconsideration that would prevent the allowance of the application, the Examiner contact the undersigned attorney to address those issues before subsequent action is taken.

§ 102 and § 103 Rejections

Claims 23, 26-27, 30-31, 34-35, 38-39, 41 and 44 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2005/0102264 ("Nason").

Claims 1-2, 5-8, 11-13, 16-20, 40, 42, 45, 48-50 and 52 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason, in view of U.S. Patent Application Publication No. 2002/0136408 ("Garcia").

Claims 3-4, 14-15 and 46-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Garcia, in further view of U.S. Patent No. 5,727,062 ("Ritter").

Claims 9-10 and 20-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Garcia, in further view of U.S. Patent No. 5,572,235 ("Mical").

Claims 24-25, 32-33 and 43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Ritter.

Claims 28-29 and 36-37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Mical.

Claim 51 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Garcia, in further view of U.S. Patent No. 6,934,389 ("Strasser").

Claims 53-56, 59, 63-66, 69-73, 76, 80-83 and 86 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser.

Claims 87, 89-92 and 93-94 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Garcia, in further view of Strasser.

Claims 57-58, 74-75 and 88 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser, in further view of Ritter.

Claims 60-62 and 77-79 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser, in further view of Garcia.

Claims 60-62 and 77-79 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser, in further view of Garcia.

Claims 67-68 and 84-85 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nason in view of Strasser, in further view of Mical.

The Claims

Claim 1 recites a method comprising:

- decrypting encrypted data that resides on one or more memory surfaces associated with a video card, said act of decrypting being performed under the influence of ***a cryptographic processor that resides on the video card***, said act of decrypting taking place only when an operation is to be performed on the data by ***a graphics processor unit (GPU) that resides on the video card***;

- ***performing an operation on the decrypted data using the GPU to provide resultant data***;
- ***re-encrypting, under the influence of the cryptographic processor, the resultant data***; and
- writing the encrypted resultant data to a memory surface associated with the video card.
- ***at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis***. (***Emphasis added.***)

In making out the rejection of this claim, the Office argues that its subject matter rendered obvious by the combination of Nason with Garcia. Applicant respectfully disagrees and traverses the Office's rejection. For the reasons set forth below, the rejection over the combination of Nason and Garcia does not establish a *prima facie* case of obviousness.

The proposed combination of references fails to disclose the claimed subject matter. Further, portions of Garcia relied upon are not enabling with respect to the claimed subject matter. Additionally motivation for the proposed combination of references is lacking because the references teach away from the proposed combination and/or the proposed combination would result in an impermissible modification of one or more of the references. Detailed arguments for each of these points are presented in the following discussion.

A. Failure to Disclose Claimed Subject Matter

The Office argues that Nason discloses essentially all of the subject matter of claim 1, except for the act of "decrypting being performed under the influence of a cryptographic processor that resides on the video card". *Office Action dated*

12/07/06 p. 18. For this feature, the Office relies on Garcia. Applicant respectfully disagrees. The Office is in error with respect this point as described below.

Nason at paragraph [0056], which describes FIG. 7, is relied upon for "at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis" as recited in claim 1. Applicant respectfully disagrees. Nason is completely devoid of any teachings or suggestion related to an act of "decrypting or re-encrypting on a per cache page basis". For example, Nason makes no mention whatsoever of a "cache page", "cache", or any of their respective equivalents. More to the point, Nason expresses no concern at all for any cache (of a GPU or otherwise) or any operations performed in such a context. Paragraph [0056] of Nason addresses moving portions of a frame in VRAM and masking a portion with an already obfuscated portion. This apparently occurs outside of any obfuscation/deobfuscation. Thus, Nason in the cited portion teaches measures that are performed with respect to secure **portions** of information, eventually resident in VRAM, under the control of an SEDD. Nasson lacks disclosure indicating that decrypting or re-encrypting, assuming this occurs, is performed on a per cache page basis. For instance, Nason is silent on how or if element 708 of FIG. 7 (obfuscated data) is decrypted or re-encrypted. Simply rearranging portions of data in memory as in FIG. 7 and paragraph [0056] of Nason is not equivalent to the claimed feature. The Office is respectfully referred to page 26, lines 1-23 of the Specification as originally filed for clarifying information in this regard.

Further, Nason fails to teach or suggest "a cryptographic processor that resides on the video card" as positively recited in claim 1. The office acknowledges this point and instead relies upon Garcia.

However, Garcia fails to cure the deficiencies of Nason. Specifically, Garcia fails to teach or suggest "a cryptographic processor that resides on the video card" as positively recited by this claim. Rather, Garcia teaches **particular** encryption algorithms of variable block lengths, as applied to graphical data *Garcia Abstract, paragraphs [0036]-[0041]*. Garcia then briefly mentions that these specific algorithms (the focus and intent of Garcia) can be implemented by way of, for example, "graphics cards with encryption facilities", and "Graphic Processing Unit (GPU) devices with encryption facilities". *Garcia, paragraphs [0074]-[0075].* However, Garcia does not provide any insight as to particular embodiments or respective details of the forgoing. In fact, Garcia fails to mention a cryptographic processor at all. Examiner relies upon a statement from the scope portion of Garcia which indicates:

> These algorithms **open the door to a new device** which making use of the GPU capabilities, combines graphic and cryptographic functions at low cost, and therefore this device **would have a great demand** providing easy cryptography (without loading the CPU) to PC (Personal Computers) all over the world guaranteeing secure communications conducted either in any intranet of in the world-wide net. *Garcia, p. 1 paragraph [0003].*

Respectfully, this portion of Garcia indicates only that **the door is open** for a new device which "combines graphic and cryptographic functions". A cryptographic

processor is not mentioned, nor is a cryptographic processor that resides on the video card. Cryptographic functions do not equate to a cryptographic processor. Further, the passage states that "the door is open to a new device" based on the algorithms presented in Garcia and is not understood as indicating that such new devices are available in the art at the time of the disclosure. For instance, the statement "this device **would** have a great demand" is forward looking. Accordingly, applicant disagrees that this portion of Garcia provides a basis for "a cryptographic processor that resides on the video card" as recited in claim 1. Accordingly, since the Office has already acknowledged that Nason lacks "decrypting being performed under the influence of a cryptographic processor that resides on the video card", the proposed combination fails to disclose, teach or suggest, this recited feature of claim 1.

There is no way to select elements from Nason, and then to somehow combine those elements with other elements taken from Garcia, in order to arrive at the subject matter recited by claim 1, as no possible combination of Nason and Garcia teaches or suggests all of the required features. At the very least, any such combination of Nason and Garcia is completely lacking: 1) a video card including a graphics processor unit and a cryptographic processor resident thereon; 2) re-encrypting, under the influence of the cryptographic processor, resultant data from an operation of the GPU; and 3) any operation performed on a per cache page basis.

Accordingly, the Office's *prima facie* case of obviousness fails for at least the reason that the combination of Nason and Garcia fails to teach or suggest all of the features recited in the claimed subject matter. For at least the foregoing reasons the references of record fail to disclose all the recited features of claim 1. Accordingly claim 1 is allowable for at least this reason.

B. Garcia is not enabling with respect to features of claim 1 for which the refrence is cited.

The Office is respectfully referred to MPEP 2121.01, which states, in pertinent part:

> "The disclosure in an assertedly anticipating reference must provide an **enabling disclosure** of the desired subject matter; **mere naming or description of the subject matter is insufficient, if it cannot be produced without undue experimentation.** *Elan Pharm., Inc. v. Mayo Found. For Med. Educ. & Research*, 346 F.3d 1051, 1054, 68 USPQ2d 1373, 1376 (Fed. Cir. 2003)." (**Emphasis added.**)

In view of the foregoing provisions of the MPEP, the Applicant asserts that Garcia is lacking sufficient enablement to serve as an enabling (i.e., sufficient) reference as Garcia has been applied by the Office. As noted, Garcia does describe that the door is open for a new device which "combines graphic and cryptographic functions". However, no details are offered regarding such a device. One of skill in the art is provided with no guidance from Garcia on how to make and use "a new device which making use of the GPU capabilities, combines graphic and cryptographic" as in Garcia, let alone a "cryptographic processor that resides on the video card" for which it is cited. Garcia simply

asserts that the specific algorithms taught thereby – and does not suggest that any others - are suitable for implementation by such casually mentioned means. Such nebulous hinting by Garcia is in stark contrast to the particular teachings of the pending Application, especially at Figs. 5 and 6 of the Drawings, and at page 17, line 15 to page 20, line 15 of the Specification, as respectively originally filed. Garcia is exclusively concerned with particular algorithms for providing secured data content in a specific way. Thus, Garcia is lacking in sufficient enablement with respect to the features of claim 1 for which it is relied upon.

C. Motivation to Combine is Lacking because The References Teach Away from the Proposed Combination.

As the examiner is no doubt aware, motivation to combine is lacking when the references teach away from the proposed combination.

Nason specifically teaches methods and systems for preventing the unauthorized access, interception and/or modification of computer code on a client device and, among other things, such data as pertaining to graphical information resident in VRAM of a video card (Abstract, *et seq.* of Nason). However, it is important to note that under every procedure or method taught by Nason - pertinent in any way to information resident on a video card - a Security Enhanced Display Driver (SEDD) plays an essential role in the "scheduling" (i.e., control, derivation, provision and/or exchange) of secured data. For example, Nason recites:

> "In one embodiment, **a security enhanced display driver (SEDD)** is provided to schedule content of portions of a frame buffer stored in a video display memory. In one such embodiment, a request to display data to a secure region on a video display made to **the SEDD**. In response, **the SEDD allocates** a corresponding secure portion of the frame buffer and **schedules** the data content of this secure portion such that valid data is only present in the secure portion at the time it is needed for projection to the display device and when other tasks are locked out of accessing (reading or writing) to the secure portion. The SEDD **determines**, depending upon, the obfuscation techniques used, when data stored in the secure portion needs to be de-obfuscated and when it needs to be re-obfuscated. *Nason, paragraph [0011].*

Nason in another passage indicates:

> the security enhanced drivers (SEDs) 406 preferably reside between the operating system device drivers 405 and the hardware so as to better control secure processing of input and output in the lowest layers of a computing system. *Nason, paragraph [0043].*

Thus, Nason groups the SEDD together within all other drivers, software and the operating system used by the client computer to be kept secure (Fig. 1 of Nason). Nason further makes it clear that the operating system, display driver (i.e., SEDD), and other software reside and are utilized by a processor **away from** both the video card and any VRAM resident thereon (Figs. 2 and 4 of Nason).

In contrast Garcia expresses a desire to limit involvement of external processing such as by the client or the CPU. For instance, in the above excerpted portion Garcia states: "These algorithms open the door to a new device which making use of the GPU capabilities, combines graphic and cryptographic

functions at low cost, and therefore this device would have a great demand providing easy cryptography **(without loading the CPU)**" (emphasis added). Thus, Garcia apparently seeks to segregate the cryptographic functions to new devices (combined with the GPU) which are away from the CPU, while, Nason exclusively teaches that: 1) an SEDD is not part of any video card; yet is 2) essential to any and all security measures taken with respect to a video card; and 3) resides between the operating system device drivers and the hardware. Thus, the SEDD (a software component) of Nason acts as an intermediate between the client and hardware which is not consistent with Garcia which seeks to provides algorithms for cryptographic functions in hardware. To this extent, Nason and Garcia teach directly away from their proposed combination.

D. Impermissible Modification to Principle of Operation

Assuming *arguendo* that Nason, when combined with Garcia, *does* teach all of the required features (which it does not), the Office attempts an impermissible modification to the teachings of Nason in order to arrive at the subject matter of claim 1.

To begin, the Applicant asserts that Nason contemplates **only** those security measures that are implemented by way of conventional, widely-known video card technology under the control of a security-enhanced driver (SEDD), and that such is fundamental to the principle of operation of the Nason teachings. That is, the SEDD of Nason operates by way of a corresponding microprocessor of the client

computer from a location **off** the video card. Thus, the Applicant further contends, any encrypted or decrypted data under Nason is derived by way of microprocessor operations separate and apart from any video card, wherein such data is subsequently communicated to such a video card.

The Office then asserts (wrongly) that, in view of the teachings of Garcia, it would be obvious to:

> modify the method disclosed in Nason et al. to incorporate the cryptographic processor within the GPU which is located on the graphics card. This modification would have been obvious because a person having ordinary skill in the art, at the time the invention was made, would have been motivated to do so since Garcia suggests that incorporating cryptographic capabilities within the GPU make performing cryptographic functions easier and is not costly." *Office Action dated 12/7/06, p.18.*

This is assertion is flawed, and any modifications to Nason there under are impermissible, for at least the following reasons:

1) Nason, as explained above, *exclusively* teaches methods and systems founded on a conventional video card under the control of a proprietary driver – namely, an SEDD. Thus, the any modification to Nason resulting in the shifting of the performance of such security measures (encryption, decryption, etc.), or any other related operations, from off-card SEDD control to a cryptographic processor on a video card constitutes a fundamental and material change in the operating principle of Nason, that is neither taught nor suggested by the Nason reference. In view of MPEP § 2143.01(VI), such a change is not allowed and an assertion for *prima facie* obviousness cannot be supported thereby.

2) The motivation for the proposed modification expressed by the Office has no bearing on, and is neither taught nor suggested by, the concerns discussed within Nason. Specifically, Nason expresses no concern with respect to the cost of implementing the sort of security features (i.e., the SEDD) taught thereby. Likewise, Nason expresses no concern for the ease of implementation of the SEDD or any related driver. Thus, there is no motivation to be found anywhere within Nason to suggest that less costly or easier-to-implement solutions should be pursued. From all indications - or rather, the complete lack thereof - Nason is fully satisfied as to the economy and straightforwardness of the solutions presented therein.

3) As explained above, neither Nason nor Garcia teaches or suggests the particular sort of cryptographic processor needed in order to perform the subject matter as recited by claim 1. Furthermore, neither Nason nor Garcia teaches or suggests all of the particular operations as recited by the subject matter of claim 1. Thus, *even if* there were legitimate support within Nason to permit the sort of modifications thereto asserted by the Office (which there is not), neither Nason nor Garcia provides, teaches or suggests the overall specific, synergistic form and functionality that would be required.

Accordingly, the Office's *prima facie* case of obviousness fails for at least the reason that the proposed modifications to the teachings of Nason are impermissible and lacking adequate support within Nason and Garcia. For at least the foregoing reasons, the Applicant asserts that claim 1 is allowable.

Claims 2-11 are allowable at least as depending from an allowable base claim. While the particular rejections against claims 2-11 have been considered, none are seen as expressing anything of merit.

Claim 12 recites a method comprising:

- ***decrypting encrypted data*** that resides on one or more memory surfaces associated with a video card, ***said act of decrypting being performed under the influence of a cryptographic processor that resides on the video card***, said act of decrypting taking place only when an operation is to be performed on the data by a graphics processor unit (GPU) that resides on the video card;
- performing an operation on the decrypted data using the GPU to provide resultant data;
- ***re-encrypting, under the influence of the cryptographic processor, the resultant data***; and
- ***writing the encrypted resultant data to a memory surface associated with the video card***;
- ***said acts of decrypting and re-encrypting taking place on a per cache page basis***. (***Emphasis added.***)

In making out the rejection of this claim, the Office argues that its subject matter is rendered obvious by the combination of Nason with Garcia. Applicant respectfully disagrees and traverses the Office's rejection. For the reasons set forth below, the rejection over the combination of Nason and Garcia does not establish a *prima facie* case of obviousness.

The proposed combination fails to disclose the claimed subject matter. Further, portions of Garcia relied upon are not enabling with respect to the claimed subject matter. Additionally motivation for the proposed combination of references is lacking because the references teach away from the proposed combination and/or the proposed combination would result in an impermissible

modification of one or more of the references. The Office is respectfully directed to the reasons argued above in regard to claim 1, as such are analogous and supportive in regard to claim 12.

In the first place, Nason neither teaches nor suggests "decrypting encrypted data . . . said act of decrypting being performed under the influence of a cryptographic processor that resides on the video card" as positively recited by the subject matter of claim 12. The Office has admitted to this deficiency of Nason. Nason further fails to teach or suggest "re-encrypting, under the influence of the cryptographic processor, the resultant data" and "writing the encrypted resultant data to a memory surface associated with the video card" as positively recited by the subject matter of claim 12. Furthermore, Nason fails to teach or suggest "said acts of decrypting and re-encrypting taking place on a per cache page basis" as positively recited by the subject matter of this claim.

Garcia fails to cure the deficiencies of Nason. Specifically, Garcia fails to teach or suggest "decrypting encrypted data . . . said act of decrypting being performed under the influence of a cryptographic processor that resides on the video card" as positively recited by the subject matter of claim 12. Again, Garcia teaches on those specific algorithms of interest to Garcia, and then briefly suggests (without enabling detail) means for performing such particular algorithms – nothing more. Furthermore, Garcia fails to teach or suggest any of: "re-encrypting, under the influence of the cryptographic processor, the resultant data" or "said acts of decrypting and re-encrypting taking place on a per cache page

basis" as respectively and positively recited by the subject matter of claim 12. Therefore, no possible combination of Nason with Garcia teaches or suggests all of the features of the subject matter of claim 12.

Secondly, *even if* some combination of Nason with Garcia taught or suggested all of the required elements (and in fact, no such combination exists), motivation for the proposed combination is lacking because the references teach away from the combination and an impermissible change in the operating principle of Nason would be required. Again, the Office is respectfully directed to the reasons argued above in regard to claim 1, as such are analogous and supportive in regard to claim 12.

For at least the foregoing reasons, the §103 rejection of claim 12 is unsupportable and must be withdrawn. The Applicant asserts that clam 12 is allowable.

Claims 13-22 are allowable at least as depending from an allowable base claim. While the particular rejections against claims 13-22 have been considered, none are seen as expressing anything of merit.

Claim 23 recites a method comprising:

- decrypting encrypted data that resides on one or more memory surfaces of a video card memory, said act of decrypting taking place only when an operation is to be performed on the data by a graphics processor unit (GPU) that resides on the video card;
- performing an operation on the decrypted data using the GPU to provide resultant data;
- re-encrypting the resultant data; and
- writing the encrypted resultant data to a video card memory surface associated with the video card,

- ***at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis. (Emphasis added)***

In making out the rejection of this claim, the Office argues that its subject matter is anticipated by Nason. Applicant respectfully disagrees and traverses the Office's rejection. For the reasons set forth below, the rejection over Nason does not support a rejection based on anticipation.

Specifically, Nason fails to provide "at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis" as positively recited by the subject matter of claim 23. Nason expresses no concern for any sort decrypting and/or re-encrypting performed on a per cache page basis.

For at least the foregoing reasons, Nason fails to provide at least one feature as positively recited by this claim. Accordingly, the anticipation rejection of claim 23 is unsupportable and must be withdrawn. In turn, claim 23 is allowable.

Claims 24-30 are allowable at least as depending from an allowable base claim. While the particular rejections against claims 24-30 have been considered, none are seen as expressing anything of merit.

Claim 31 recites a method comprising:

- decrypting encrypted data that resides on one or more memory surfaces of a video card memory, said act of decrypting taking place only when an operation is to be performed on the data by a graphics processor unit (GPU) that resides on the video card;
- performing an operation on the decrypted data using the GPU to provide resultant data;
- re-encrypting the resultant data; and
- writing the encrypted resultant data to a video card memory surface associated with the video card,

- ***said acts of decrypting and re-encrypting taking place on a per cache page basis. (Emphasis added)***

In making out the rejection of this claim, the Office argues that its subject matter is anticipated by Nason. Applicant respectfully disagrees and traverses the Office's rejection. For the reasons set forth below, the rejection over Nason does not support a rejection based on anticipation.

Specifically, Nason fail to provide "said acts of decrypting and re-encrypting taking place on a per cache page basis" as positively recited by the subject matter of claim 31. For reasons analogous to those argued above in regard to claim 12, Nason fails to provide at least one feature as positively recited by this claim. Accordingly, the anticipation rejection of claim 31 is unsupportable and must be withdrawn. In turn, claim 31 is allowable.

Claims 32-38 are allowable at least as depending from an allowable base claim. While the particular rejections against claims 32-38 have been considered, none are seen as expressing anything of merit.

Claim 39 recites a system comprising:

- ***means for decrypting, on a per cache page basis, encrypted data that resides on one or more memory surfaces of a video card memory only when an operation is to be performed on the data by a graphics processor unit (GPU) that resides on the video card***;
- means for performing an operation on the decrypted data to provide resultant data;
- means for re-encrypting, on a per cache page basis, the resultant data; and
- means for writing the encrypted resultant data to a video card memory surface associated with the video card. (***Emphasis added***)

In making out the rejection of this claim, the Office argues that its subject matter is anticipated by Nason. Applicant respectfully disagrees and traverses the Office's rejection. For the reasons set forth below, the rejection over Nason does not support a rejection based on anticipation.

Specifically, Nason fails to provide "means for re-encrypting, on a per cache page basis, the resultant data" as positively recited by the subject matter of this claim. As argued above, Nason makes no provision for any means for, nor any procedure regarding anything performed on a per cache page basis. For at least these reasons, Nason fails to provide at least one feature as positively recited by this claim. Accordingly, the anticipation rejection of claim 39 is unsupportable and must be withdrawn. In turn, claim 39 is allowable.

Claims 40-44 are allowable at least as depending from an allowable base claim. While the particular rejections against claims 40-44 have been considered, none are seen as expressing anything of merit.

Claim 45 recites a system comprising:

- a video card;
- a graphics processor unit (GPU) on the video card and configured to process video data that is to be rendered on a display device;
- ***memory on the video card comprising*** one or more input memory surfaces configured to hold encrypted data that is to be operated upon by the GPU, and ***one or more output memory surfaces configured to hold encrypted resultant data*** that is to be rendered on the display device;
- ***a cryptographic processor on the video card and configured to control encryption and decryption on the video card***, the cryptographic processor being configured to enable encrypted data on one or more of the input memory surfaces to be decrypted, on a

per cache page basis, in connection with an operation that is to be performed on the data by the GPU; and

- ***the cryptographic processor further being configured to enable data that has been operated upon by the GPU to be encrypted, on a per cache page basis, to an output memory surface. (Emphasis added)***

In making out the rejection of this claim, the Office argues that its subject matter is rendered obvious by the combination of Nason with Garcia. Applicant respectfully disagrees and traverses the Office's rejection. For the reasons set forth below, the rejection over the combination of Nason and Garcia does not establish a *prima facie* case of obviousness.

The proposed combination fails to disclose the claimed subject matter. Further, portions of Garcia relied upon are not enabling with respect to the claimed subject matter. Additionally motivation for the proposed combination of references is lacking because the references teach away from the proposed combination and/or the proposed combination would result in an impermissible modification of one or more of the references. The Office is respectfully directed to the reasons argued above in regard to claim 1, as such are analogous and supportive in regard to claim 45.

Nason fails to teach or suggest "a cryptographic processor on the video card and configured to control encryption and decryption on the video card" as positively recited by the subject matter of this claim. Such deficiency on the part of Nason has been admitted by the Office. Also, Nason fails to teach or suggest "the cryptographic processor further being configured to enable data that has been

operated upon by the GPU to be encrypted, on a **per cache page basis**, to an output memory surface" as positively recited by the subject matter of this claim. Nason is lacking any teachings regarding any operation or means going to a "per cache page basis". Frankly, Nason is directed to substantially different means and methods of operation, than the subject matter as recited by claim 45.

Garcia fails to cure the deficiencies of Nason. Specifically, Garcia fails to teach or suggest "a cryptographic processor on the video card and configured to control encryption and decryption on the video card" as positively recited by the subject matter of this claim. As argued above, Garcia makes only broad, off-hand suggestions as to the means to be employed to perform the specific algorithms of Garcia. Garcia does not teach or suggest the particular "cryptographic processor" nor its configuration, as recited by the subject matter of claim 45. Also, Garcia is lacking any teachings or suggestions directed to "the cryptographic processor further being configured to enable data that has been operated upon by the GPU to be encrypted, on a per cache page basis, to an output memory surface" as positively recited by the subject matter of this claim. Therefore, no possible combination of Nason and Garcia provides all of the features as recited by the subject matter of claim 45.

Further, assuming for the sake of argument only that Nason and Garcia are combinable to produce all the recited features of claims 45 (which they are not), motivation for the proposed combination is lacking because the references teach away from their combination and an impermissible change in the operating

principle of Nason would be required. Again, the Office is respectfully directed to the reasons argued above in regard to claim 1, as such are analogous and supportive in regard to claim 45.

For at least the forgoing reasons, the Office has failed to support a *prima facie* obviousness rejection against claim 45. Therefore, the Applicant asserts that claim 45 is allowable.

Claims 46-52 are allowable at least as depending from an allowable base claim. While the particular rejections against claims 46-52 have been considered, none are seen as expressing anything of merit.

Claim 53 recites a method comprising:

- providing multiple input memory surfaces that are to hold encrypted data that is to be processed by a graphics processor unit (GPU) on a video card;
- ***associating, with each input memory surface, a decryptor that is uniquely configured so as to decrypt the encrypted data that is held by the associated input memory surface***;
- decrypting, with at least one associated decryptor, encrypted data that resides on at least one respective input memory surface;
- ***performing an operation on the decrypted data using the GPU to provide resultant data***;
- ***re-encrypting the resultant data***; and
- ***writing the encrypted resultant data to an output memory surface associated with the video card***,
- ***at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis. (Emphasis added)***

In making out the rejection of this claim, the Office argues that its subject matter rendered obvious by the combination of Nason with Strasser. Applicant respectfully disagrees and traverses the Office's rejection. For at least the reasons

set forth below, the rejection over the combination of Nason and Strasser does not establish a *prima facie* case of obviousness.

Nason fails to teach or suggest "associating, with each input memory surface, a decryptor that is uniquely configured so as to decrypt the encrypted data that is held by the associated input memory surface" as positively recited by the subject matter of this claim. The Office has already acknowledged this deficiency on the part of Nason. *Office Action dated 12/7/06, p.37.* It is important to note that the operating principles of Nason are such that decryptors are not associated each input memory surface – an SEDD of Nason is used exclusively to perform or cause any encryption and/or decryption of data. The Office is respectfully referred to Fig. 3, and page 13, lines 15-25 of the pending Application for exemplary detail in this regard.

Also, Nason fails to teach or suggest "performing an operation on the decrypted data using the GPU to provide resultant data" and "re-encrypting the resultant data" as positively recited by the subject matter of this claim. Nason includes no teachings directed to the re-encrypting of "resultant data" from a (previous) operation of a GPU. Also, Nason is devoid of any method comprising "at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis" as positively recited by the subject matter of this claim.

Strasser fails to cure the deficiencies of Nason. Specifically, Strasser fails to teach or suggest "associating, with each input memory surface, a decryptor that is uniquely configured so as to decrypt the encrypted data that is held by the

associated input memory surface" as positively recited by the subject matter of this claim. On this point, the Office asserts that Strasser teaches "using keys which are unique to each data stream for content encryption/decryption protects the content from eavesdroppers". *Office Action dated 12/7/06, p.37.* Respectfully, this is not the same as, or suggestive of, the subject matter of claim 53.

More particularly, Strasser expresses no concern for memory surfaces or uniquely configured decryptors associated with each. Strasser is concerned with the frequent (i.e., every two seconds) provision of new CP keys within a dynamic data stream between two entities (Col. 4, lines 2-9 of Strasser), **not** the maintaining of data security on a memory surface (i.e., data that is not being presently communicated between entities). Furthermore, Strasser fails to teach or suggest "performing an operation on the decrypted data using the GPU to provide resultant data" and "re-encrypting the resultant data" as positively recited by the subject matter of this claim. Strasser is still further deficient in failing to teach or suggest "at least one of said acts of decrypting and re-encrypting taking place on a per cache page basis" as positively recited by claim 53.

Accordingly, the Office's *prima facie* case of obviousness fails for at least the reasons that: 1) no combination of Nason with Strasser teaches or suggest all of the required features; and 2) the proposed modifications to the teachings of Nason are impermissible and lacking adequate support within Nason and Strasser. For at least the foregoing reasons, the Applicant asserts that claim 53 is allowable.

Claims 54-69 are allowable at least as depending from an allowable base claim. While the particular rejections against claims 54-69 have been considered, none are seen as contributing anything of merit.

Claim 70 recites a method comprising

- providing multiple input memory surfaces that are to hold encrypted data that is to be processed by a graphics processor unit (GPU) on a video card;
- ***associating, with each input memory surface, a decryptor that is uniquely configured so as to decrypt the encrypted data that is held by the associated input memory surface***;
- decrypting, with at least one associated decryptor, encrypted data that resides on at least one respective input memory surface;
- ***performing an operation on the decrypted data using the GPU to provide resultant data***;
- ***re-encrypting the resultant data***; and
- ***writing the encrypted resultant data to an output memory surface associated with the video card,***
- ***said acts of decrypting and re-encrypting taking place on a per cache page basis. (Emphasis Added.)***

In making out the rejection of this claim, the Office argues that its subject matter rendered obvious by the combination of Nason with Strasser. Applicant respectfully disagrees and traverses the Office's rejection. For at least the reasons set forth below, the rejection over the combination of Nason and Strasser does not establish a *prima facie* case of obviousness.

Specifically, no possible combination of Nason with Strasser teaches or suggests any of: 1) "associating, with each input memory surface, a decryptor that is uniquely configured so as to decrypt the encrypted data that is held by the associated input memory surface" 2) "performing an operation on the decrypted

data using the GPU to provide resultant data" 3) "re-encrypting the resultant data; and writing the encrypted resultant data to an output memory surface associated with the video card" or 4) "said acts of decrypting and re-encrypting taking place on a per cache page basis" as respectively and positively recited by the subject matter of claim 70.

The Applicant asserts that the arguments provided above at least in support of claim 53 are analogous and supportive of claim 70. Additionally, the proposed modifications to the teachings of Nason are impermissible and lacking adequate support within Nason and Strasser. For at least the foregoing reasons, the Applicant asserts that claim 70 is allowable.

Claims 71-86 are allowable at least as depending from an allowable base claim. While the particular rejections against claims 71-86 have been considered, none are seen as contributing anything of merit.

Claim 87 recites a system comprising:

- a video card;
- ***a graphics processor unit (GPU) on the video card*** and configured to process video data that is to be rendered on a display device;
- memory on the video card comprising one or more input memory surfaces configured to hold encrypted data that is to be operated upon by the GPU, and one or more output memory surfaces configured to hold encrypted resultant data that is to be rendered on the display device;
- ***a cryptographic processor on the video card and configured to control encryption and decryption on the video card, the cryptographic processor comprising a key manager for managing keys that can be utilized for encrypting and decrypting data on the video card***;
- each individual input memory surface having its own unique associated key for decrypting encrypted data held thereon;

- ***the cryptographic processor being configured to enable encrypted data on one or more of the input memory surfaces to be decrypted on a per cache page basis*** so that the decrypted data can be operated upon by the GPU;
- the cryptographic processor further being configured to enable ***data that has been operated upon by the GPU to be encrypted on a per cache page basis*** to an output memory surface. (***Emphasis Added)***

In making out the rejection of this claim, the Office argues that its subject matter rendered obvious by the combination of Nason with Garcia and Strasser. Applicant respectfully disagrees and traverses the Office's rejection. For at least the reasons set forth below, the rejection over the combination of Nason, Garcia and Strasser does not establish a *prima facie* case of obviousness.

Specifically, Nason fails to teach or suggest "a graphics processor unit (GPU) on the video card" and "a cryptographic processor on the video card and configured to control encryption and decryption on the video card" as positively recited by the subject matter of this claim. The Office has admitted to this deficiency of Nason. Nason additionally fails to teach or suggest the "cryptographic processor comprising a key manager for managing keys that can be utilized for encrypting and decrypting data on the video card" as positively recited by the subject matter of this claim. Nason also fails to teach or suggest "the cryptographic processor being configured to enable encrypted data on one or more of the input memory surfaces to be decrypted on a per cache page basis" as positively recited by the subject matter of claim 87. Further, Nason fails to teach or suggest "data that has been operated upon by the GPU to be encrypted on a per cache page basis" as positively recited by the subject matter of this claim.

The Office argues that Garcia teaches such a "cryptographic processor" because (according to the Office) Garcia teaches "that incorporating cryptographic capabilities within the GPU has many added benefits". *Office Action dated 12/7/06, p.45*. However, and as argued above, any means mentioned by Garcia for executing the algorithms thereof are passing at best, and are completely lacking any specificity or detail on the order of the subject matter recited by claim 87. In any case, Garcia does not cure the deficiencies on the part of Nason with respect to the "cryptographic processor" and/or any of its specific capabilities as recited by claim 87.

In turn, Strasser fails to cure the mutual deficiencies of Nason and Garcia. In particular, Strasser fails to teach or suggest "the cryptographic processor being configured to enable encrypted data on one or more of the input memory surfaces to be decrypted on a per cache page basis" as positively recited by the subject matter of claim 87. Further still, Strasser fails to teach or suggest "data that has been operated upon by the GPU to be encrypted on a per cache page basis" as positively recited by the subject matter of this claim.

Strasser is not concerned with the particular structure and cooperative aspects of the subject matter of claim 87 because, among other things, Strasser is direct to solving a different problem (i.e., providing secure communication between remote entities) in a different way (i.e., frequent provision of new encryption keys in the data streams) than the subject matter of claim 87. Furthermore, Strasser is completely lacking any teachings or suggestions directed

to means or operations performed on a "per cache page basis". More to the point, Strasser is totally devoid of the terms "cache", "cache page", or any of their respective equivalents, in any context.

There is no way select elements from Nason, and then to combine those with other elements selected from Garcia, and then to combine those with still other elements selected from Strasser, in order to arrive at the subject matter as recited by claim 87, as no possible combination of Nason, Garcia and Strasser teaches or suggests all of the required features. On these grounds alone, the Applicant contends that the § 103 rejection of claim 87 is unsupportable, and must be withdrawn.

Additionally, no teachings or elements to be found anywhere in Garcia and/or Strasser override the fact that any modification to the teachings of Nason are impermissible as any such modification would result in changing the operating principle of Nason in violation of MPEP § 2143.01(VI). Thus, to modify the teachings of Nason so as to "incorporate the cryptographic processor within the GPU which is located on the graphics card", as suggested by the Office (page 33 of Office action), is not allowable and cannot be used to support a rejection of claim 87 under § 103.

Accordingly, the Office's *prima facie* case of obviousness fails for at least the reasons that: 1) no combination of Nason with Garcia and Strasser teaches or suggest all of the required features; and 2) the proposed combination is lacking motivation as the references teach away from the proposed combination and

would result in impermissible modifications to Nason. For at least the foregoing reasons, the Applicant asserts that claim 87 is allowable.

Claims 88-94 are allowable at least as depending from an allowable base claim. While the particular rejections against claims 88-94 have been considered, none are seen as contributing anything of merit.

Conclusion

The Application is in a condition for allowance. The Applicant respectfully requests reconsideration and issuance of the present application. Should any issue remain that prevents immediate issuance of the application, the Examiner is requested to contact the undersigned attorney to discuss the unresolved issue.

Respectfully submitted,

Dated: 2/7/07

By: /Daniel T. McGinnity, #55,444/

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